REMARKS

Claims 1-8 were examined and reported in the Office Action. Claims 1, 2, 4 and 6-8 are rejected. Claims 1-4 and 6-8 are amended. New claims 9-12 are added. Claims 1-12 remain.

Applicants request reconsideration of the application in view of the following remarks.

I. Claim Objections

It is asserted in the Office Action that claims 3-6 are objected to for various formalities. Applicant has amended claims 3 and 6 to overcome the informal claim objections.

Accordingly, withdrawal of the claim objections for claims 3-6 is respectfully requested.

II. 35 U.S.C. § 112

It is asserted in the Office Action that claims 4, 6, 7 and 8 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant has amended claims 4, 7 and 8 to overcome the 35 U.S.C. § 112, second paragraph rejections.

Accordingly, withdrawal of the 35 U.S.C. § 112 second paragraph rejections for claims 4, 6, 7 and 8 are respectfully requested.

III. 35 U.S.C. § 102(e)

It is asserted in the Office Action that claims 1, 2 and 7 are rejected in the Office Action under 35 U.S.C. § 102(e), as being anticipated by U. S. Patent No. 6,557,080 issued to Burger ("Burger"). Applicant respectfully traverses the aforementioned rejection for the following reasons.

According to MPEP §2131,

> '[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a

> single prior art reference.' (Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)). 'The identical invention must be shown in as complete detail as is contained in the ... claim.' (Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)). The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, *i.e.*, identity of terminology is not required. (In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)).

Applicant's amended claim 1 contains the limitations of

> ... a cell area having N+1 number of unit cell blocks, each including M number of word lines which respectively are coupled to a plurality of unit cells wherein the N number of unit cell blocks are corresponded to logical cell block addresses and one unit cell block is added for accessing data with high speed; a predetermined cell block table for assigning M number of word lines among the (N+1) x M number of the word lines as predetermined restorable word lines; a tag block having N+1 number of unit tag blocks, each unit tag block storing at least one physical cell block address storing data wherein the tag block receives a logical cell block address designated for accessing one of N number of unit cell blocks and converts the logical cell block address into a physical cell block address designated for accessing one of the N+1 number of unit cell blocks; and a control means for activating one word line of a unit cell block selected by the physical cell block address and a corresponding one of the predetermined restorable word lines by controlling the tag block and the predetermined cell block table, wherein the tag block stores information representing an update of the logical cell block address and a refresh operation is preformed through the use of the information.

Applicant's amended claim 7 contains the limitations of

> [a] method for a refresh operation of a semiconductor memory device including a cell area having N+1 number of unit cell blocks, each including M number of word lines which respectively are coupled to a plurality of unit cells; a predetermined cell block table for assigning M number of word lines among (N + 1) x M number of the word lines as predetermined restorable word lines; and a tag block for storing a physical cell block address, the tag block having N+1 number of unit tag blocks, each having M number of registers for sensing an update of data, wherein one word line of a unit cell block selected by the physical cell block address and a

> corresponding one of the predetermined restorable word lines are activated, comprising the steps of: (A) starting a refresh mode; (B) detecting word lines determined by the physical cell block address having data by checking (N + 1) x M number of registers in the tag block, each register storing a logical block address and an information representing update of the logical block address; and (C) performing the refresh operation through the use of the information, wherein the N number of unit cell blocks are corresponded to addresses and one unit cell block is added for accessing data with high speed.

Burger discloses a cache structure that allows dynamic control of the size and configuration of a data block fetched by the cache from the memory. It is asserted in the Office Action that a cache 16 shown in Fig. 1 of Burger corresponds to a cell area 510 having (N+1) number of unit cell blocks shown in Fig. 5 of Applicant's claimed invention. In Burge, the cache 16 (or a memory 14) includes M (number of word lines) × N (number of unit cell blocks) word lines. Distinguishable, in Applicant's claimed invention, the cell area 510 includes (N+1) x M word lines.

In particular, the cell area 510 of Applicant's claimed invention includes M more word lines as predetermined restorable word lines, which are not fixed but changed during an operation of a semiconductor memory device. Accordingly, as shown in Fig. 4 of Applicant's claimed invention, the semiconductor memory device can activate two word lines, which are one word line of a unit cell block selected by a physical cell block address and a corresponding one of the predetermined restorable word lines located at another unit cell block. Even if data stored in one of two activated word lines are sensed and amplified, the other of two activated word lines still stores data. As a result, a data access time of the semiconductor memory device can actually preclude a data restoration time, and thus, the data access time can effectively be reduced to obtain high speed operation of the semiconductor memory device.

Further, it is asserted in the Office Action that a tag memory 28 illustrated in Fig. 1 of Burger corresponds to a tag block 530 shown in Fig. 5 of Applicant's claimed invention. In Burger, however, the tag memory 28 only holds a tag for distinguishing data output from a memory address range 22 of the memory 14 when data is stored in the cache 16.

Distinguishable, in Applicant's claimed invention the tag block 530 not only holds a tag (i.e., a logical cell block address corresponding to N number of unit cell blocks), but also information representing an update of the logical cell block address. Therefore, the information represents which one of the above two activated word lines has real data. Thus, the semiconductor memory device performs a refresh operation by using the information. As a result, the refresh operation is only performed for the word line having the real data. Thus, operation time of the refresh operation is reduced.

Burger does not teach, disclose or even suggest the cell area having (N+1) x M word lines in order to reduce the data access time by activating two word lines, and the tag block for storing the information representing which one of the above two activated word lines has real data.

Therefore, Burger does not disclose, teach or suggest Applicant's claim 1 limitations of

> a cell area having N+1 number of unit cell blocks, each including M number of word lines which respectively are coupled to a plurality of unit cells wherein the N number of unit cell blocks are corresponded to logical cell block addresses and one unit cell block is added for accessing data with high speed; a predetermined cell block table for assigning M number of word lines among the (N+1) x M number of the word lines as predetermined restorable word lines; a tag block having N+1 number of unit tag blocks, each unit tag block storing at least one physical cell block address storing data wherein the tag block receives a logical cell block address designated for accessing one of N number of unit cell blocks and converts the logical cell block address into a physical cell block address designated for accessing one of the N+1 number of unit cell blocks; and a control means for activating one word line of a unit cell block selected by the physical cell block address and a corresponding one of the predetermined restorable word lines by controlling the tag block and the predetermined cell block table, wherein the tag block stores information representing an update of the logical cell block address and a refresh operation is preformed through the use of the information,

nor Applicant's claim 7 limitations of

> a predetermined cell block table for assigning M number of word lines among (N + 1) x M number of the word lines as

> predetermined restorable word lines; and a tag block for storing a physical cell block address, the tag block having N+1 number of unit tag blocks, each having M number of registers for sensing an update of data, wherein one word line of a unit cell block selected by the physical cell block address and a corresponding one of the predetermined restorable word lines are activated.

Therefore, since Burger does not disclose, teach or suggest all of Applicant's amended claims 1 and 7 limitations, Applicant respectfully asserts that a *prima facie* rejection under 35 U.S.C. § 102(e) has not been adequately set forth relative to Burger. Thus, Applicant's amended claims 1 and 7 are not anticipated by Burger. Additionally, the claim that directly depends on amended claim 1, namely claim 2, is also not anticipated by Burger for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 102(e) rejections for claims 1, 2 and 7 are respectfully requested.

IV. 35 U.S.C. § 103(a)

It is asserted in the Office Action that claim 8 is rejected in the Office Action under 35 U.S.C. § 103(a), as being unpatentable over Burger in further view of U. S. PG Publication No. 2002/0141272 issued to Benedix et al ("Benedix"). Applicant respectfully traverses the aforementioned rejection for the following reasons.

According to MPEP §2142

> [t]o establish a prima facie case of obviousness, three basic c riteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the kno wledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. S econd, there must be a reasonable expectation of success. Fi nally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reas onable expectation of success must both be found in the prio r art, and not based on applicant's disclosure. (In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)).

Further, according to MPEP §2143.03, "[t]o establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)." "*All words in a claim must be considered* in judging the patentability of that claim against the prior art." (In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970), emphasis added.)

Applicant's amended claim 8 directly depends on amended claim 7. Applicant has addressed Burger regarding amended claim 7 above in section III.

Benedix discloses a dynamic semiconductor memory. The memory of Benedix includes a control device. In the event of an external refresh command, the control device causes, after the refresh operation, the state of the memory banks to be reestablished. That is, the word line whose address was stored in the register is reactivated. As with Burger, Benedix does not disclose, teach or suggest Applicant's claim 7 limitations of

> a predetermined cell block table for assigning M number of word lines among (N + 1) x M number of the word lines as predetermined restorable word lines; and a tag block for storing a physical cell block address, the tag block having N+1 number of unit tag blocks, each having M number of registers for sensing an update of data, wherein one word line of a unit cell block selected by the physical cell block address and a corresponding one of the predetermined restorable word lines are activated.

Since neither Burger, Benedix, and therefore, nor the combination of the two, teach, disclose or suggest all the limitations of Applicant's amended claim 7, as listed above, Applicant's amended claim 7 is not obvious over Burger in view of Benedix since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claim that directly depends from amended claim 7, namely claim 8, would also not be obvious over Burger in view of Benedix for the same reason

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejection for claim 8 is respectfully requested.

V. Claims Not Rejected Over Prior Art

Applicant notes with appreciation the Examiner's assertion that claims 3 and 5 are not rejected over prior art.

Applicant respectfully asserts that claims 1-12, as they now stand, are allowable for the reasons given above.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending, namely 1-12, patentably define the subject invention over the prior art of record and are in condition for allowance and such action is earnestly solicited at the earliest possible date.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly extension of time fees. If a telephone interview would expedite the prosecution of this Application, the Examiner is invited to contact the undersigned at (310) 207-3800.

Respectfully submitted,

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Dated: October 13, 2006

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail with sufficient postage in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P. O. Box 1450, Alexandria, Virginia 22313-1450 on October 13, 2006.

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Jean Svoboda